PATENT
Docket No.: 16869C-017000US
Client Ref. No.: HAL-ID 150

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	
John Simons	Examiner: Qamrun Nahar
Application No.: 09/747,824	Art Unit: 2124
Filed: December 22, 2000	
For: Assembly Language Code Compilation for an Instruction-Set Architecture Containing New Instructions Using the Prior Assembler	**Declaration of John Simons**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, JOHN SIMONS, declare as follows:

1. I am the inventor of the technology described and claimed in this patent application. I have spoken with an attorney for Hitachi, the assignee of my patent application, who has explained to me that the application is being rejected under 35 U.S.C. § 102(c) because the invention was abandoned. I submit this declaration to explain the facts and circumstances behind the delay between the reduction to practice in about 1994 and the filing of the application in 2000.

2. In 1994 a research team within Hitachi was involved in adding new instructions to perform digital signal processing to an existing microprocessor product. I understood the new design would require a new assembler. This new assembler would need to recognize and assemble to machine language, the assembly language instructions for the instruction set architecture used by the original processor. The new assembler would also need to recognize and assemble to machine language, the new DSP instructions that were contemplated for addition to the processor.

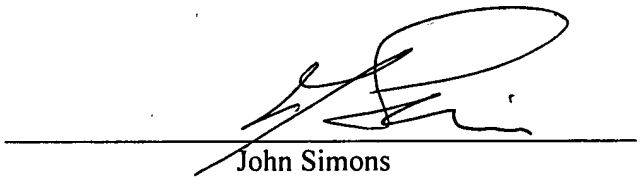
3. I used the techniques described in my patent application to allow the group to benchmark various instructions. At the completion of the project, I did not think these techniques would be useful in the future because I did not think the processors involved

in our work would be extended in the future. In addition, once the processor design was finalized, Hitachi created a new compiler which compiled all of the instructions, and that compiler was provided to customers for the new DSP extended microprocessor. My understanding at that time was that Hitachi planned to do a new assembler for each new product, and therefore the techniques of my invention were of no further use.

4. The technique I developed was not considered again for use until the year 2000 when a request was made to me to investigate another extension of this processor. This was the first extension considered for the instruction set after the 1994 project. Furthermore, the difficulties of adding more features to that microprocessor design were not really appreciated until the year 2000. When this new challenge was presented, I remembered the technique I used in 1994 to study the DSP instructions. I then proceeded to use that same technique to study potential new instructions for the next generation processor. It was at this time that I realized the usefulness of this technique. Once I realized that usefulness, this patent application was filed.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: May 28, 2004



John Simons